REMARKS

Claims 1-17 are presented for further examination. Claims 1-5, 7, 9, and 14 have been amended.

In the final Office Action mailed April 21, 2004, the Examiner objected to claims 1, 5, and 9 for lack of antecedent basis. Applicant has amended these claims to overcome this objection.

Claims 1-17 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,054,024 ("Whetsel"). Remarks accompanying this rejection state that Whetsel teaches more than one dedicated clock signal, *e.g.*, TCK, DTCK.

Applicant respectfully disagrees and requests reconsideration and further examination of the claims. The Examiner refers to Figure 2, Element 74 of Whetsel as teaching a respective dedicated clock. However, as applicant previously argued on page 8, last paragraph, of the previous Amendment, reference number 74 is for a TMS SEL CKT test mode selection circuit that outputs device test mode selection signals 1-4 in response to a test mode select and optional test mode select signal received via input buffers 24, 82 respectively. Whetsel teaches reception of a single clock signal TCK that is received at the TMS SEL CKT 74 and is also sent to an output DTCK. There is only one clock signal generated by a single clock signal generator that is off circuit with respect to the device select module (DSM). In fact, Whetsel teaches using a new object called a DSM plus a remote bus master 12 from which the clock signal TCK is sent.

More particularly, the present invention includes a plurality of clock generators; each clock generator generating a dedicated clock signal for a respective TAP function. Nowhere does Whetsel teach or suggest a plurality of clock generators. The TMS SEL CKT 74 of Whetsel is not a clock generator. Rather, it receives the single TCK signal on line 80.

Applicant notes that Figure 1 shows a plurality of DSM devices (18a, 18b), but each of these devices receives a single clock signal TCK from the primary bus master 12. There is no teaching or suggestion of using a plurality of clock generators on the single chip for generating a dedicated clock signal for respective TAP functions.

Claim 1 recites, *inter alia*, generating a clock signal for each component of the plurality of components using a dedicated clock generator for each clock signal. Nowhere does

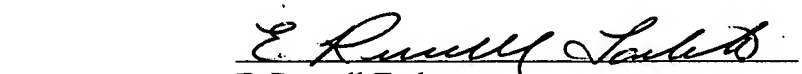
Whetsel teach or suggest a dedicated clock generator for each clock signal for each of the plurality of components.

Independent claim 5 recites a plurality of clock generators on the single chip, each dedicated clock generator generating a dedicated clock signal for selectively driving a respective TAP function in a respective component of the plurality of components. Similar limitations are found in independent claims 9 and 14. In view of the foregoing, applicant respectfully submits that all of these independent claims and all claims depending therefrom are clearly allowable over Whetsel. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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